

WHAT IS CLAIMED IS:

- 1 1. A programmable logic device comprising:
2 a plurality of logic array blocks;
3 a programmable interconnect bus, programmably coupled to the
4 plurality of logic array blocks;
5 a tristate bus; and
6 a plurality of tristate devices, coupled between the plurality of logic
7 array blocks and the tristate bus, wherein the plurality of tristate devices couple and decouple
8 the logic array blocks to the tristate bus.

- 1 2. The programmable logic device of claim 1 further comprising:
2 a plurality of OE generation circuits, coupled to the plurality of tristate
3 devices, the plurality of OE generation circuits controlling the plurality of tristate devices.

- 1 3. The programmable logic device of claim 2 wherein a logic array block
2 programmably couples to drive the plurality of OE generation circuits.

- 1 4. The programmable logic device of claim 1 further comprising:
2 a tristate bus driver, coupled between the tristate bus and the
3 programmable interconnect bus, for driving signals between the tristate bus and
4 programmable interconnect bus.

- 1 5. A programmable logic device comprising:
2 a programmable interconnect bus; and
3 a logic array block, comprising:
4 a plurality of logic elements configurable to perform logical functions;
5 a plurality of tristate drivers, coupled between the plurality of logic
6 elements and the programmable interconnect bus; and
7 tristate control logic controlling states of the plurality of tristate
8 drivers.

- 1 6. The programmable logic device of claim 5 wherein the plurality of
2 tristate drivers are programmably enabled to couple the plurality of logic elements to the
3 programmable interconnect bus.

1 7. The programmable logic device of claim 5 wherein the tristate control
2 logic is programmably coupled to signals on the programmable interconnect bus for
3 controlling the states of the plurality of tristate drivers.

1 8. The programmable logic device of claim 5 wherein one of the plurality
2 of logic elements is coupled through one of the plurality of tristate drivers through the
3 programmable interconnect bus to another one of the plurality of logic elements.

1 9. A tristate driver for an integrated circuit comprising:
2 a data input;
3 an enable control node;
4 a first driver transistor, coupled between a first potential source and an
5 output node;
6 a second driver transistor, coupled between the output node and a
7 second potential source;
8 a first predriver comprising:
9 a first transistor, coupled between the first potential source and a
10 control electrode of the first driver transistor, having a control electrode coupled to an
11 inversion of the enable input;
12 a second transistor, coupled between the control electrode of the first
13 electrode driver transistor and control of the second driver transistor, having a control
14 electrode coupled to the inversion of the enable input; and
15 a third transistor, coupled between the control electrode of the second
16 driver transistor and the second potential source, having a control electrode coupled to the
17 enable input; and
18 a second predriver comprising:
19 a first transistor, coupled between the first potential source and the
20 control electrode of the first driver transistor, having a control electrode coupled to the data
21 input;
22 a second transistor, coupled between the control electrode of the first
23 driver transistor and the control electrode of the second driver transistor, having a control
24 electrode coupled to the enable input; and

25 a third transistor, coupled between the control electrode of the second
26 driver transistor and the second potential source, having a control electrode coupled to the
27 data input.